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TEC GUIDANCE FOR STUDENTS

Contents

TECHNICIAN EDUCATION COUNCIL

Certificate Programme in Telecommunications

Sets of model questions and answers for Technician Education Council (TEC) units are given below. The questions illustrate the types of questions that students may encounter, and are useful as practice material for the skills learned during the course.

Where additional text is given for educational purposes, it is shown within square brackets to distinguish it from information expected of students under examination conditions. Representative time limits are shown for each question, and care has been taken to give model answers that reflect these limits.

We would like to emphasise that the questions are not representative of questions set by any particular college.

TEC: ELECTRICAL AND ELECTRONIC PRINCIPLES III

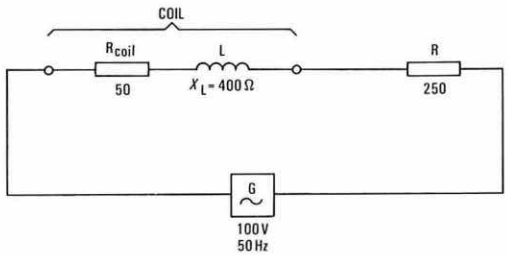
TEC unit number U81/742. Students are advised to read the notes above

Students should allow about 6 min for each question in section A and 30 min for each question in section B.

SECTION A

Q1 *A coil having an inductive reactance of 400 Ω and a resistance of 50 Ω is connected in series with a 250 Ω resistor across a 100 V 50 Hz supply (see circuit diagram).*

Calculate the potential difference across the coil.



A1 The total resistance, R_T,

$$= R_{coil} + R = 50 + 250 = 300\ \Omega.$$

The total impedance, Z,

$$= \sqrt{(R_T^2 + X_L^2)},$$

where X_L is the reactive impedance of the coil.

$$\therefore \quad Z = \sqrt{(300^2 + 400^2)} = 500\ \Omega.$$

The current, I,

$$= \frac{100}{500} = 0{\cdot}2\ \text{A}.$$

The impedance of the coil, Z_{coil},

$$= \sqrt{(R^2_{coil} + X_L^2)},$$

$$= \sqrt{(50^2 + 400^2)} = 403{\cdot}1\ \Omega.$$

Therefore, the potential difference across the coil

$$= I \times Z_{coil} = 0{\cdot}2 \times 403{\cdot}1,$$

$$= \underline{80{\cdot}62\ \text{V}}.$$

Q2 *A low-loss parallel circuit, consisting of a coil and a variable capacitor set to 12 pF, is tuned to resonate at 450 kHz. The bandwidth of the circuit is 9 kHz.*

If the capacitance is increased to 48 pF, determine the new values of

(a) the resonant frequency, and

(b) the bandwidth.

A2 [*Tutorial note:* As this is a low-loss circuit, the resonant frequency, f_r, can be taken as

$$f_r = \frac{1}{2\pi\sqrt{(LC)}},$$

where L is the inductance and C is the capacitance.]

(*a*) The resonant frequency, f_r, $= \dfrac{1}{2\pi\sqrt{(LC)}}$.

The initial resonant frequency, f_{r1},

$$= \frac{k_1}{\sqrt{C_1}} = 450\ \text{kHz},$$

where k_1 is a constant for this circuit equal to $1/(2\pi\sqrt{L})$, and C_1 is the initial capacitance.

The final resonant frequency, f_{r2},

$$= \frac{k_1}{\sqrt{(4C_1)}} = \tfrac{1}{2} \times \frac{k_1}{\sqrt{C_1}} = \frac{f_{r1}}{2},$$

$$= \underline{225\ \text{kHz}}.$$

(*b*) The magnification factor, Q, is given by

$$Q = \frac{1}{2\pi f_r CR},$$

where R is the resistance.

The initial magnification factor, Q_1,

$$= \frac{1}{2\pi f_{r1} C_1 R} = \frac{k_2}{f_{r1} C_1},$$

where the constant k_2 is $1/(2\pi R)$.

The final magnification factor, Q_2,

$$= \frac{k_2}{f_{r2} \times 4C_1},$$

$$= \frac{k_2}{\frac{f_{r1}}{2} \times 4C_1} \text{ (since } f_{r2} = f_{r1}/2),$$

$$= \frac{k_2}{2f_{r1}C_1},$$

$$= \frac{Q_1}{2}.$$

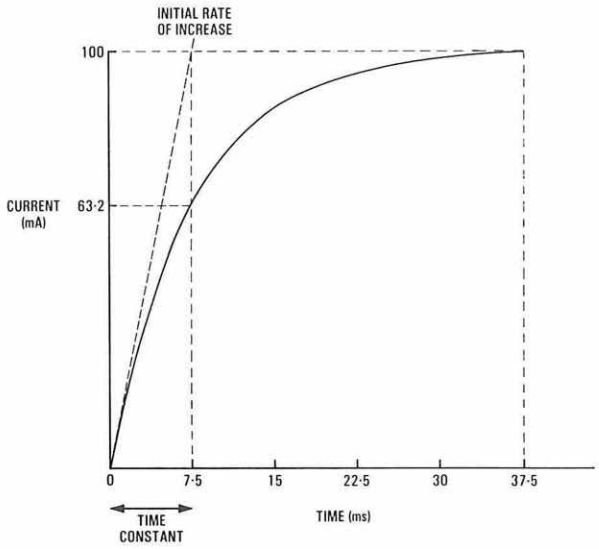
The initial bandwidth, B_1,

$$= \frac{f_{r1}}{Q_1} = 9 \text{ kHz}.$$

The final bandwidth, B_2,

$$= \frac{f_{r2}}{Q_2} = \frac{f_{r1}/2}{Q_1/2} = \frac{f_{r1}}{Q_1},$$

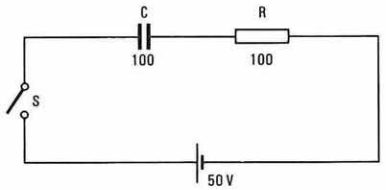
$$= \underline{9 \text{ kHz}}.$$



Q3 The 100 μF capacitor shown in the circuit diagram is initially fully discharged. For the instant that switch S is closed, calculate

(a) the current flowing through resistor R, and

(b) the rate of increase of the potential difference across capacitor C.



A3 (*a*) Initially, the charge held by the capacitor, $q = 0$ C.
Therefore, the potential difference across the capacitor, v_C,

$$= \frac{q}{C} = 0 \text{ V}.$$

The applied voltage, V,

$$= v_C + v_R,$$

where v_R is the initial potential difference across resistor R.
Therefore, v_R is equal to the applied voltage, $V = 50$ V.
Therefore, the initial current

$$= \frac{v_R}{R} = \frac{50}{100} = \underline{0{\cdot}5 \text{ A}}.$$

(*b*) The time constant, T,

$$= CR = 100 \times 10^{-6} \times 100 = 10 \times 10^{-3} \text{ s}.$$

[*Tutorial note:* If the capacitor continued charging at its initial rate, it would be fully charged in a time equal to the time constant.]
Therefore, the initial rate of increase of potential difference

$$= \frac{V}{CR} = \frac{50}{10 \times 10^{-3}},$$

$$= \underline{5000 \text{ V/s}}.$$

Q4 A coil having an inductance (L) of 15 H and a resistance (R) of 2000 Ω is connected in series with a switch across a 200 V supply (V).
Show, by means of a sketch graph, the variation of the current through the coil from the instant the switch is closed. Indicate on your graph the significance of the circuit time constant.

A4 The time constant

$$= \frac{L}{R} = \frac{15}{2000} = 7{\cdot}5 \text{ ms}.$$

The final steady current

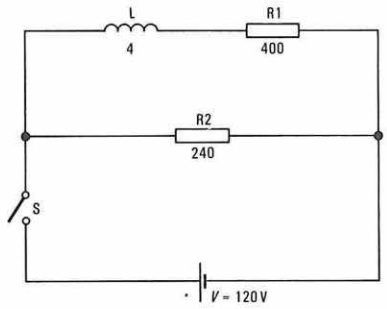
$$= \frac{V}{R} = \frac{200}{2000} \text{ A} = 100 \text{ mA}.$$

The graph is shown opposite.

Q5 Switch S in the circuit shown below has been closed for a significant time. Calculate for the instant that switch S is opened:

(a) the potential difference across resistor R2, and

(b) the EMF induced in the inductance L.



A5 (*a*) Before switch S is opened, the current through inductance L

$$= \frac{V}{R_1} = \frac{120}{400} = 0{\cdot}3 \text{ A}.$$

At the instant switch S is opened, the current through inductance L $= 0{\cdot}3$ A.

[*Tutorial note:* The current through the inductance cannot change instantaneously. The path for this current is through inductance L and resistors R1 and R2.]

Therefore, the current through resistor R2 $= 0{\cdot}3$ A.
Therefore, the potential difference across resistor R2

$$= 0{\cdot}3 \times 240,$$

$$= \underline{72 \text{ V}}.$$

(*b*) The instantaneous EMF induced in inductance L when switch S is opened must be sufficient to enable an instantaneous current of $0{\cdot}3$ A to flow through resistors R1 and R2.
Therefore, the EMF induced in inductance L

$$= 0{\cdot}3 \times (400 + 240) = 0{\cdot}3 \times 640,$$

$$= \underline{192 \text{ V}}.$$

Q6 An ideal transformer is required to supply a 48 V 120 W load from a 240 V 50 Hz supply. If the primary winding of the transformer has 400 turns, calculate:

(a) the number of turns on the secondary winding,

(b) the current flowing in the secondary circuit, and

(c) the current flowing in the primary circuit.

A6 Let the number of turns on the primary and secondary windings be N_p and N_s, the supply and load voltages be V_p and V_s, and the supply and load currents be I_p and I_s, respectively.

(*a*) $$\frac{N_s}{N_p} = \frac{V_s}{V_p}.$$

$$\therefore \quad N_s = N_p \times \frac{V_s}{V_p} = 400 \times \frac{48}{240},$$

$$= \underline{80 \text{ turns.}}$$

(*b*) The output power, P_{out}, $= V_s I_s$.

$$\therefore \quad I_s = \frac{P_{out}}{V_s} = \frac{120}{48} = \underline{2{\cdot}5 \text{ A.}}$$

(*c*) The input power = the output power.

$$\therefore \quad V_p I_p = P_{out}.$$

$$\therefore \quad I_p = \frac{P_{out}}{V_p} = \frac{120}{240},$$

$$= \underline{0{\cdot}5 \text{ A.}}$$

Q7 A transformer is required to operate at a frequency of 450 kHz in a small-signal radio-frequency amplifier.
Suggest a suitable core material. Explain why the material is suitable and how it minimises core losses.

A7 A suitable core material is ferrite.
Ferrite has a sufficiently high permeability to provide the required inductance without the component being unduly large.
The core losses to be minimised are:

(*a*) hysteresis loss—the energy lost when the core is taken through cycles of magnetisation, and

(*b*) eddy-current loss—the energy lost because of circulating curents in the core.

The type of ferrite used would have a very narrow hyteresis loop (that is, low remanence and low coercivity) to keep hysteresis losses to a minimum.
The very high resistivity of ferrite makes it particularly suitable for minimising eddy-current losses.

Q8 A 220 V DC motor is required to produce an output torque of 10 N m and a shaft speed of 1500 rev/min.
If the efficiency of the motor is 85%, determine the required supply current.

A8 The output power, P_{out}, is given by

$$P_{out} = \frac{2\pi NT}{60} \text{ watts,}$$

where N is the motor speed (1500 rev/min) and T is the torque (10 N m).

$$\therefore \quad P_{out} = \frac{2\pi \times 1500 \times 10}{60},$$

$$= 1570{\cdot}8 \text{ W.}$$

The efficiency, η, is given by

$$\eta = \frac{P_{out}}{P_{in}} \times 100\%,$$

where P_{in} is the input power.

$$\therefore \quad P_{in} = P_{out} \times \frac{100}{\eta},$$

$$= 1570{\cdot}8 \times \frac{100}{85},$$

$$= 1848 \text{ W.}$$

But, $$P_{in} = V_s I_s,$$

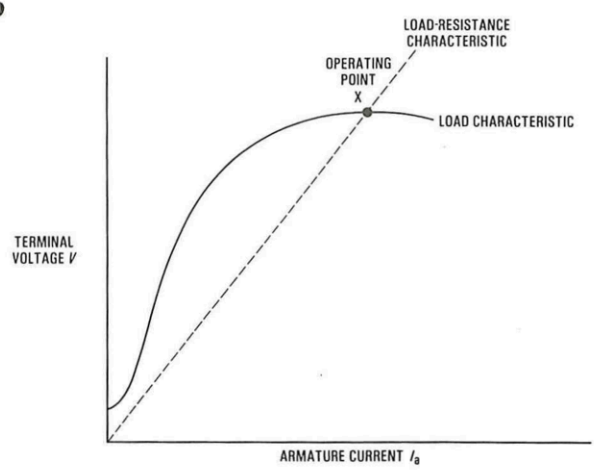
where V_s and I_s are the supply voltage and current, respectively.

$$\therefore \quad I_s = \frac{P_{in}}{V_s} = \frac{1848}{220},$$

$$= \underline{8{\cdot}4 \text{ A.}}$$

Q9 Sketch the load characteristic for a series-wound DC generator.
Show, with the aid of the load characteristic, how the operating conditions can be determined for a particular resistive load.

A9



In a series-wound generator, the load current is equal to the armature current. The operating condition is determined by plotting the load-resistance (R_L) characteristic using the following relationship:

$$V = I_a R_L.$$

The load-resistance characteristic is shown as a dotted line in the sketch. The intersection of the 2 characteristics at point X indicates the operating condition of the generator.

Q10 When a DC shunt motor operates at a speed of 1500 rev/min, it generates a back EMF of 210 V. The load on the motor is increased until the back EMF falls to 154 V. Calculate the motor speed for the new load condition.

A10 The back EMF, E, is proportional to $N \times \Phi$, where N is the motor speed and Φ is the flux produced by the shunt field.

$$\therefore \quad \frac{E}{N} \propto \Phi.$$

In a shunt motor the field flux, Φ, remains constant.

$$\therefore \quad \frac{E}{N} = \text{constant.}$$

Let E_1 and N_1 represent the initial condition, and E_2 and N_2 the final condition; then

$$\frac{E_1}{N_1} = \frac{E_2}{N_2}.$$

$$\therefore \quad \frac{210}{1500} = \frac{154}{N_2}.$$

$$\therefore \quad N_2 = \frac{1500 \times 154}{210},$$

$$= \underline{1100 \text{ rev/min.}}$$

SECTION B

Q11 (*a*) *A coil is connected in series with a calibrated variable capacitor across the output of a signal generator. The output voltage and frequency of the signal generator are maintained constant at 5 V and 10 kHz, respectively, throughout the test procedure.*
When the capacitance is varied, a maximum current of 40 mA flows when the capacitance is set to 8 nF.

Calculate:
(*i*) *the resistance of the coil,*
(*ii*) *the inductance of the coil,*
(*iii*) *the Q-factor of the series tuned circuit,*
(*iv*) *the maximum voltage across the capacitor,*
(*v*) *the maximum power dissipated in the circuit.*

(*b*) *Sketch, for the circuit under test, a graph showing the variation of circuit impedance with frequency.*

A11 (*a*) The circuit is resonating at 10 kHz when the value of the variable capacitance, C, is 8 nF.
(*i*) At resonance, the impedance of the circuit is equal to the resistance of the coil, R.
If V_s is the supply voltage and I_{max} is the maximum current, then

$$R = \frac{V_s}{I_{max}} = \frac{5}{40 \times 10^{-3}},$$

$$= \underline{125\ \Omega.}$$

(*ii*) At resonance, the reactance of the coil is equal to the reactance of the capacitor.

Therefore, the inductance of the coil, L, is given by

$$L = \frac{1}{(2\pi f_r)^2 C},$$

where f_r is the resonance frequency.

$$\therefore \quad L = \frac{1}{(2\pi \times 10 \times 10^3)^2 \times 8 \times 10^{-9}}\ \text{H},$$

$$= \underline{31{\cdot}66\ \text{mH.}}$$

(*iii*) $$Q = \frac{1}{R}\sqrt{\left(\frac{L}{C}\right)} = \frac{1}{125} \times \sqrt{\left(\frac{31{\cdot}66 \times 10^{-3}}{8 \times 10^{-9}}\right)},$$

$$= \underline{15{\cdot}92.}$$

(*iv*) The maximum voltage across the capacitor occurs at resonance, and is

$$QV_s = 15{\cdot}92 \times 5 = \underline{79{\cdot}6\ \text{V.}}$$

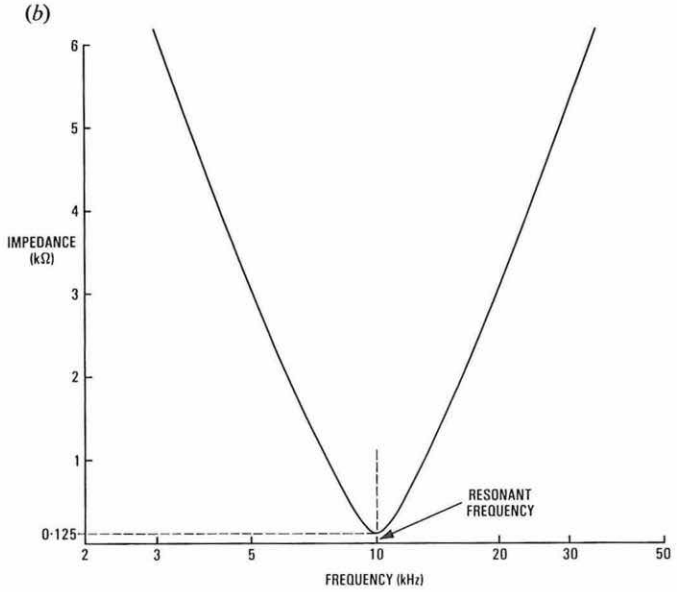
(*v*) The maximum power dissipation occurs at resonance. At resonance the signal-generator output voltage is in phase with the circuit current.

Therefore, the maximum power dissipated

$$= V_s I_{max} = 5 \times 40 \times 10^{-3}\ \text{W},$$

$$= \underline{200\ \text{mW.}}$$

(*b*)



[*Tutorial note:* A logarithmic scale has been used for the frequency axis on the sketch graph. This produces a curve almost symmetrical about the resonant frequency.]

Q12 *A 240 V 50 Hz induction motor produces a power output of 480 W at an efficiency of 80%. The power factor of the circuit is 0·7.*

(*a*) *Calculate:*

(*i*) *the supply current, and*

(*ii*) *the apparent power required by the motor.*

(*b*) *Determine the parallel capacitance required to improve the power factor to 0·95.*

A12 (*a*) (*i*) The efficiency, η,

$$= \frac{\text{output power } (P_{out})}{\text{input power } (P_{in})} \times 100\%.$$

$$\therefore \quad P_{in} = P_{out} \times \frac{100}{\eta},$$

$$= 480 \times \frac{100}{80},$$

$$= 600\ \text{W.}$$

[*Tutorial note:* This is the true power input to the circuit.]

The power factor, $\cos\phi$, is 0·7. The true power $= VI\cos\phi$, where I is the supply current and V is the supply voltage.

$$\therefore \quad I = \frac{P_{in}}{V\cos\phi} = \frac{600}{240 \times 0{\cdot}7},$$

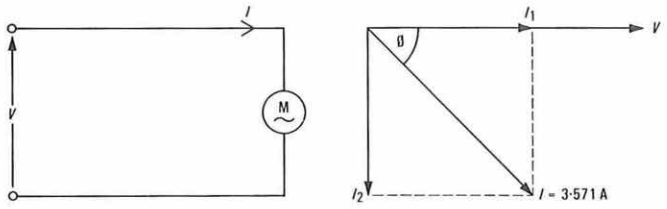
$$= \underline{3{\cdot}571\ \text{A.}}$$

(*ii*) The apparent power

$$= VI = 240 \times 3{\cdot}571,$$

$$= \underline{857\ \text{VA.}}$$

(*b*) The phasor diagram for the basic circuit (see sketch (*a*)) is shown in sketch (*b*).



(*a*) (*b*)

$$\cos\phi = 0{\cdot}7.$$

$$\therefore \quad \phi = 45{\cdot}57°.$$

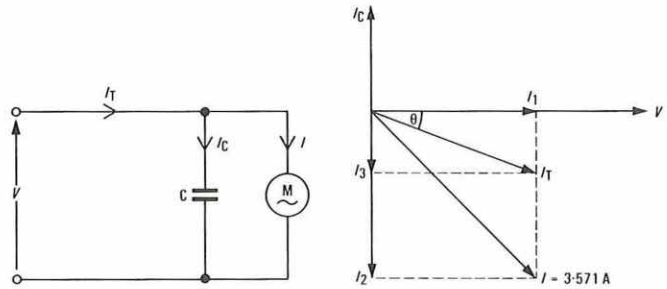
The components of I are the in-phase component, I_1,

$$= I\cos\phi = 3{\cdot}571 \times 0{\cdot}7 = 2{\cdot}5\ \text{A},$$

and the quadrature component, I_2,

$$= I\sin\phi = 3{\cdot}571 \times 0{\cdot}7141 = 2{\cdot}55\ \text{A}.$$

Sketch (*c*) shows the circuit with the parallel capacitance connected. The addition of the parallel capacitance changes the supply current to I_T. Sketch (*d*) shows the phasor diagram after the addition of the capacitor.



(*c*) (*d*)

$$\cos\theta = 0{\cdot}95.$$

$$\therefore \quad \theta = 18{\cdot}19°.$$

The components of I_T are the in-phase component, $I_1 = 2{\cdot}5$ A, and the quadrature component, I_3,

$$= I_1 \tan\theta = 2{\cdot}5 \times 0{\cdot}3287 = 0{\cdot}822\ \text{A}.$$

In order to improve the power factor to 0·95, the initial quadrature component, I_2, must be reduced to equal I_3.

$$\therefore \quad I_C = I_2 - I_3 = 2{\cdot}55 - 0{\cdot}822 = 1{\cdot}728\ \text{A}.$$

The reactance of the capacitor, X_C,

$$= \frac{V}{I_C} = \frac{240}{1{\cdot}728} = 138{\cdot}9\ \Omega.$$

But $$X_C = \frac{1}{2\pi fC},$$

where f is the frequency.

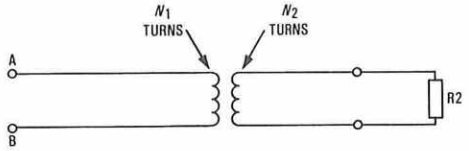
$$\therefore \quad C = \frac{1}{2\pi f X_C} = \frac{1}{2\pi \times 50 \times 138{\cdot}9}\ \text{F},$$

$$= \underline{22{\cdot}9\ \mu\text{F.}}$$

Q13 (*a*) *For the circuit shown below derive the following relationship:*

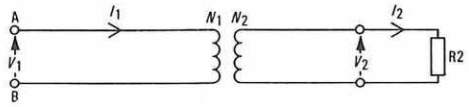
$$R_1 = R_2\left(\frac{N_1}{N_2}\right)^2,$$

where R_1 *is the input resistance at terminals A and B.*



(*b*) *Explain how a transformer can be used to match an amplifier to a load to obtain the maximum transference of power.*

A13 (*a*) See sketch (*a*).



(*a*)

$$R_1 = \frac{V_1}{I_1},$$

and

$$R_2 = \frac{V_2}{I_2}.$$

$$\therefore \quad \frac{R_1}{R_2} = \frac{\frac{V_1}{I_1}}{\frac{V_2}{I_2}},$$

$$= \frac{V_1}{I_1} \times \frac{I_2}{V_2},$$

$$= \frac{V_1}{V_2} \times \frac{I_2}{I_1}. \qquad \ldots\ldots (1)$$

But,

$$\frac{V_1}{V_2} = \frac{N_1}{N_2} = \frac{I_2}{I_1}.$$

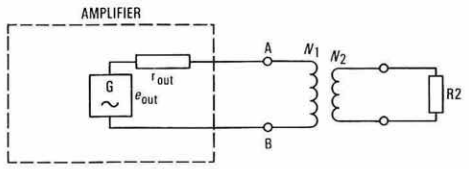
Substituting for $\frac{V_1}{V_2}$ and $\frac{I_2}{I_1}$ in equation 1,

$$\frac{R_1}{R_2} = \left(\frac{N_1}{N_2}\right)^2.$$

$$\therefore \quad R_1 = R_2\left(\frac{N_1}{N_2}\right)^2.$$

(*b*) Maximum power transfer occurs when the output resistance of the amplifier equals the amplifier load resistance.

Sketch (*b*) shows how a transformer can be used to match an amplifier to a load. The output circuit of the amplifier is represented by a voltage generator in series with the output resistance (r_{out}) of the amplifier.



(*b*)

Maximum power transfer occurs when

$$r_{out} = R_1,$$

where R_1 is the resistance presented between the terminals A and B.

The turns ratio (N_1/N_2) required for maximum power transfer is determined by substituting r_{out} for R_1 in the equation, derived in part (*a*).

Hence,

$$r_{out} = R_2\left(\frac{N_1}{N_2}\right)^2.$$

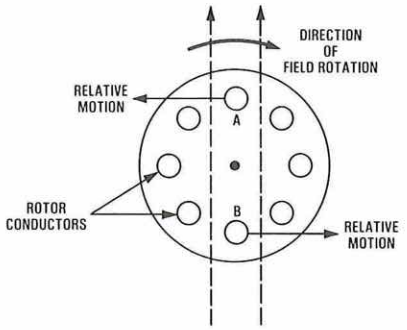
Therefore, the required turns ratio,

$$\underline{\frac{N_1}{N_2} = \sqrt{\left(\frac{r_{out}}{R_2}\right)}.}$$

Q14 (*a*) *Explain how a rotating magnetic field produces a torque in an induction motor.*

(*b*) *The synchronous speed of an induction motor is 1500 rev/min. If the percentage slip is 5%, calculate the speed of the rotor.*

A14 (*a*) An induction motor invariably has a squirrel-cage rotor; the end view of a squirrel-cage rotor is shown in sketch (*a*). All of the rotor conductors are joined at each of their ends by end rings.

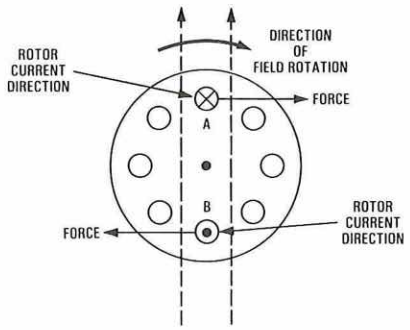


(*a*)

When the magnetic field is rotating clockwise, the relative motion of conductors A and B with respect to the rotating field is as shown in sketch (*a*). This results in EMFs being induced in conductors A and B; the directions of the EMFs are determined by using Fleming's right-hand rule.

The induced EMFs produce currents in the rotor conductors. The directions of the currents are shown in sketch (*b*).

[*Tutorial note:* The rotor conductors, together with the end rings, form complete circuits for the rotor currents.]



(*b*)

Application of Fleming's left-hand rule produces the force directions shown in sketch (*b*). The result of these forces is to produce a torque causing the rotor to rotate in the same direction as the rotating field.

(*b*)

$$\text{Percentage slip} = \frac{\text{slip speed}}{\text{synchronous speed}} \times 100.$$

$$\therefore \quad \text{slip speed} = \frac{\text{percentage slip}}{100} \times \text{synchronous speed},$$

$$= \frac{5}{100} \times 1500,$$

$$= 75 \text{ rev/min}.$$

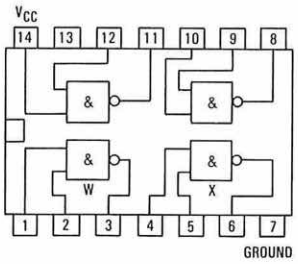
$$\text{Rotor speed} = \text{synchronous speed} - \text{slip speed},$$

$$= 1500 - 75,$$

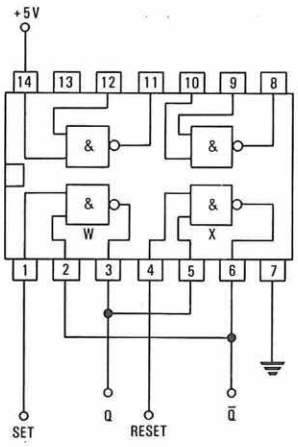
$$= \underline{1425 \text{ rev/min}}.$$

Questions and answers contributed by C. Wright

Q1 The diagram below shows the pin connections of a 7400 quad 2-input NAND gate. Copy the diagram and add to it the connections required to produce a simple RS bistable circuit. Use gates W and X. *(4 min)*



A1 A simple RS bistable circuit is shown in the sketch.



Q2 Complete the truth table given below for an RS bistable circuit which has been constructed using 2 NOR gates.

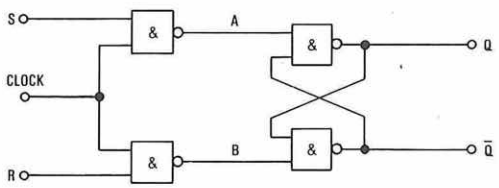
R	*S*	*Q*	$\overline{Q}$	*Comment*
0	*1*			
0	*0*			
1	*0*			
1	*1*			

(2 min)

A2

R	S	Q	$\overline{Q}$	Comment
0	1	1	0	SET condition.
0	0	1	0	Memory—retains previous state.
1	0	0	1	RESET condition.
1	1	0	0	Undesirable output since output Q has the same state as output $\overline{Q}$

Q3 For the circuit shown below, derive its truth table and briefly explain its action. *(5 min)*



A3 The circuit is a clocked RS bistable circuit, which has the following truth table:

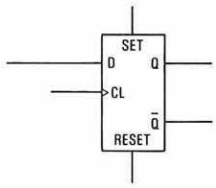
R	S	Clock	Q	$\overline{Q}$
0	1	0	Previous Q	Previous $\overline{Q}$
0	1	1	1	0
0	0	0	1	0
0	0	1	1	0
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

The clocked RS bistable circuit operates in the same way as a simple RS bistable when the clock input is at logic 1 state, but is held in its memory state whenever the clock is at logic 0.

Assuming the clock is at logic 0, then points A and B are both logic 1. Outputs Q and $\overline{Q}$ are therefore held in their previous condition by the cross-coupled connection to the other input of each NAND gate.

If the clock goes to a logic 1, the S and R inputs are inverted by the 2-input NAND gates. If, for example, the S and R inputs are logic 1 and 0, respectively, then point A is a logic 0 and point B a logic 1. This forces output Q to a logic 1 and output $\overline{Q}$ to logic 0, as indicated in the truth table.

Q4 Identify the circuit symbol and draw the sequence table to show its operation. *(2 min)*



A4 The symbol shown is for a D-type flip-flop with asynchronous SET and RESET inputs.

Its sequence table is shown below. Q_n represents the output state before the clock pulse and Q_{n+1} the state after the clock pulse.

D	Q_n	Q_{n+1}
0	0	0
1	1	1
0	1	0
1	0	1

Q5 Choose one of the answers given below to complete the sentence: A master-slave JK flip-flop . . .

(a) has an indeterminate state if the J and K inputs are both logic 0.

(b) requires 2 clock pulses to make it change state.

(c) only changes when the clock pulse is HIGH.

(d) has a toggle state if the J and K inputs are both logic 1.

(1 min)

A5 (*d*) has a toggle state if the J and K inputs are both logic 1.

Q6 Describe briefly why a master-slave JK bistable circuit is widely used in digital circuits in preference to other types of bistable circuit. *(4 min)*

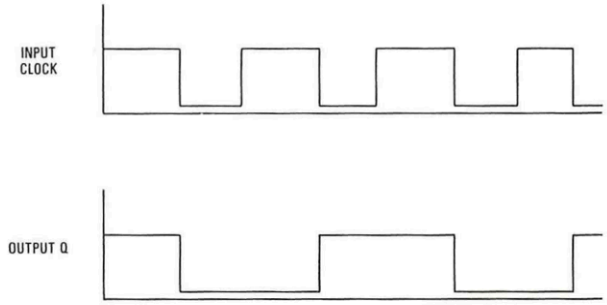
A6 The master-slave JK bistable circuit is often preferred to other types of bistable circuit for 2 main reasons:

(*a*) It has no indeterminate state, unlike the simple type of RS bistable circuit. With the JK bistable circuit, if both J and K inputs are held at logic 1, the output toggles with each clock pulse.

(*b*) The output does not change until the clock pulse has undergone a positive and negative-going transition. This ensures that in a counter circuit, for example, any feedback from the output to the input of a bistable circuit cannot affect the output until the next clock pulse.

Q7 Draw typical waveforms to illustrate the use of a master-slave JK bistable circuit as a divide-by-2 circuit. *(3 min)*

A7 The waveforms required are for the input clock and output Q and are shown in the sketch. Inputs J and K must both be held at logic 1.



The frequency of the signal at output Q is half the clock frequency, hence the term *divide-by-2*.

Q8 *Indicate whether the following statements are* TRUE *or* FALSE.

(*a*) *A synchronous counter can be used to eliminate ripple-through delay problems.*

(*b*) *Asynchronous counters are generally preferred for high-speed operation.*

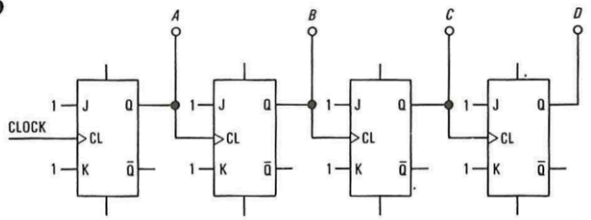
(*c*) *Only synchronous counters can be made to count down.*

(*d*) *In an asynchronous counter, the clock inputs are all connected to the common clock line.* (*2 min*)

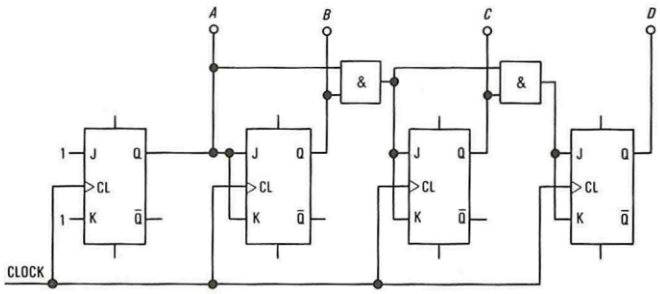
A8 (*a*) True. (*b*) False. (*c*) False. (*d*) False.

Q9 *Draw 2 circuits to illustrate the asynchronous and the synchronous forms of a divide-by-16 counter using JK bistable circuits.* (*8 min*)

A9

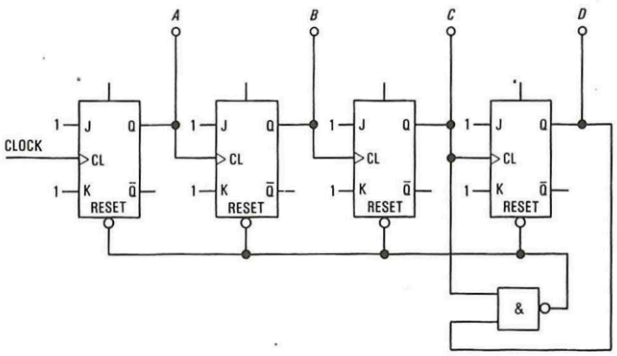


(*a*) Asynchronous divide-by-16 counter



(*b*) Synchronous divide-by-16 counter

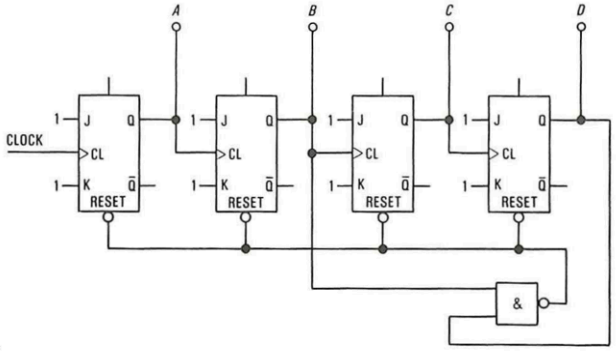
Q10 *Identify the counter illustrated below and show how it could be modified to produce a decade counter.* (*4 min*)



A10 The diagram in the question shows a divide-by-12 asynchronous counter.

When the counter reaches binary value 1100 (*D*, *C*, *B*, and *A*, respectively), it is immediately reset to 0000, so that the count begins with 0000 and ends with 1011.

The counter can be modified to form a decade counter by changing the connections to those shown in the following sketch.



Q11 *How can an asynchronous binary counter be made to count down? Draw a count sequence table to illustrate your answer.* (*5 min*)

A11 An asynchronous binary counter can be made to count down in one of two ways:

(*a*) the $\overline{Q}$ output of each bistable element can be used instead of the Q output, or

(*b*) the clock for each stage of the counter after the first can be taken from the $\overline{Q}$ output of the previous stage instead of the Q output.

The count sequence for the binary down counter is as given in the following table:

Input Clock	Outputs			
	D	*C*	*B*	*A*
0	0	0	0	0
1	1	1	1	1
2	1	1	1	0
3	1	1	0	1
4	1	1	0	0
5	1	0	1	1
6	1	0	1	0
7	1	0	0	1
8	1	0	0	0
9	0	1	1	1
10	0	1	1	0
11	0	1	0	1
12	0	1	0	0
13	0	0	1	1
14	0	0	1	0
15	0	0	0	1
16	0	0	0	0

Q12 *Which of the following statements is true?*

(*a*) *Transistor-transistor-logic (TTL) and complementary-metal-oxide-semiconductor (CMOS) counters can both operate at up to 20 MHz with a 5 V supply.*

(*b*) *CMOS counters are generally much faster than TTL counters but have higher power dissipation.*

(*c*) *The typical clock frequency of a TTL counter is 30 MHz, whereas that for a CMOS counter is only 2 MHz, with a 5 V supply.*

(*d*) *CMOS counters have lower power dissipation and higher speed than TTL counters.* (*1 min*)

A12 (*c*) The typical clock frequency of a TTL counter is 30 MHz, whereas that for a CMOS counter is only 2 MHz, with a 5 V supply.

Q13 *The CD 4045A is a 21-stage complementary-metal-oxide-semiconductor (CMOS) counter.*

(*a*) *State a typical figure for its input clock frequency.*

(*b*) *Briefly describe its count sequence.*

(*c*) *Give one typical application for such a device.* (*5 min*)

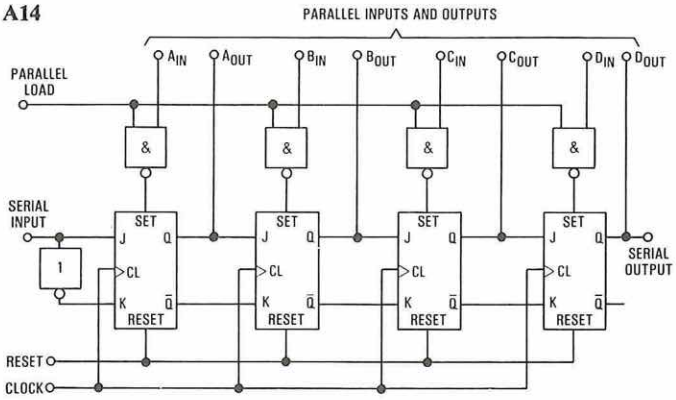
A13 (*a*) The typical clock frequency for this counter is 2 MHz with a 5 V supply. Higher input frequencies can be used if the supply voltage is increased.

(*b*) It is a binary counter with the standard sequence, but only a selection of the outputs from the bistable elements are available.

(*c*) This type of circuit is generally used as an accurate timer. For example, if the frequency of the input clock is 2·097 MHz, then the output provides a very accurate frequency of 1 pulse/s.

Q14 Draw the logic diagram of a 4-stage register showing clearly
(*a*) *serial input and output; and*
(*b*) *parallel inputs and outputs.* (*5 min*)

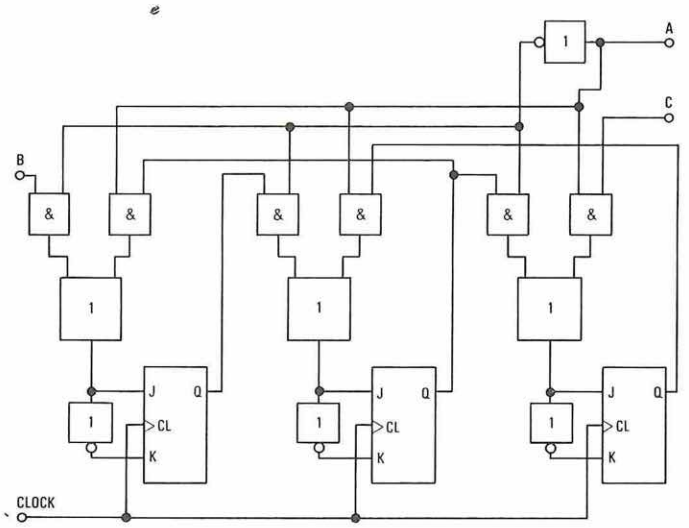
A14



Q15 Give a number of typical applications of the type of register described in Q14. (*2 min*)

A15 This type of register could be used for serial-to-parallel or parallel-to-serial data conversion. It could also be used to store binary data during a calculation.

Q16 Identify the circuit shown below, and describe what happens if points A, B and C are all held at logic 1 when clock pulses are applied. Assume that each bistable circuit is initially RESET. (*4 min*)

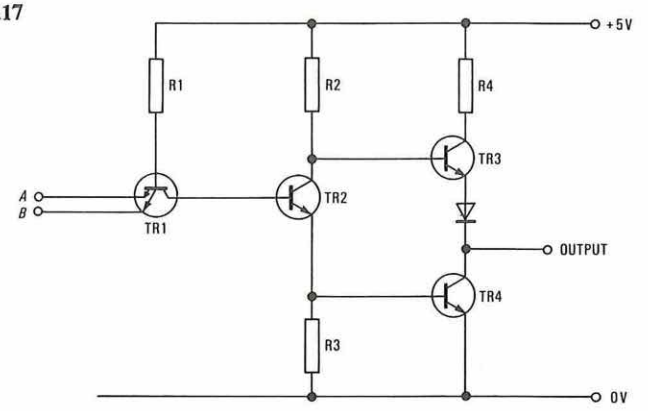


A16 The circuit shown is a 3-bit shift register with left/right shift capability. Data is entered either at input B or C, and the shift direction is controlled by input A. Logic 1 at A forces data to shift left on each clock pulse. If all 3 inputs are at logic 1, and the register is initially RESET, then the application of clock pulses causes data to shift left. The data pattern in the register is as shown in the table.

Clock	Register Data
0	0 0 0
1	0 0 1
2	0 1 1
3	1 1 1
4	1 1 1

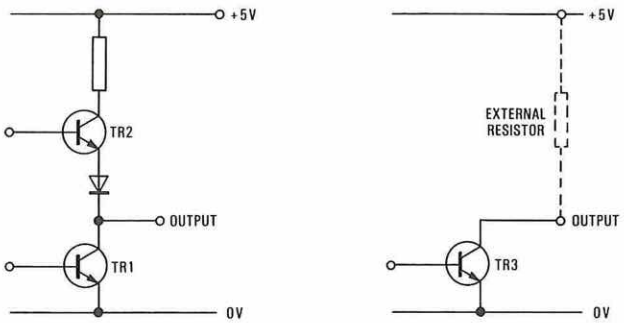
Q17 A 7400 is a quadruple 2-input transistor-transistor logic (TTL) NAND gate. Draw the circuit diagram of one of its gates. (*3 min*)

A17



Q18 Explain the difference between a 'totem pole' output stage and an open-collector output stage. Indicate where each one may be used. (*5 min*)

A18 The 2 types of output stage are shown in sketches (*a*) and (*b*).



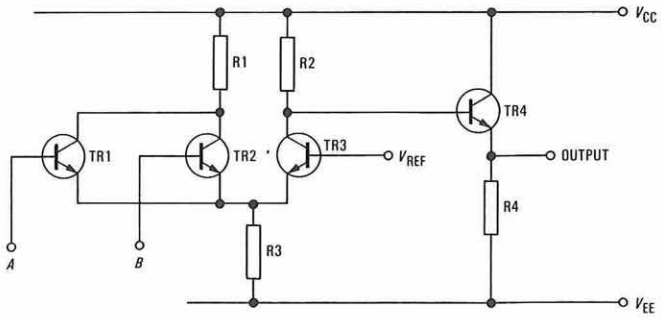
(*a*) Totem-pole output stage (*b*) Open-collector output stage

The totem pole output stage is the standard configuration for most transistor-transistor-logic circuits. When transistor TR1 saturates and TR2 is OFF, the output is pulled down to about 0·2 V, giving a logic 0 output. When transistor TR1 is OFF and transistor TR2 conducts, the output rises to about 3·5 V, which is a logic 1.

In the open-collector output stage, a connection is required between the output and supply before it will operate. This is generally a resistor known as the *pull-up resistor*. When the transistor conducts, the output falls to about 0·2 V, as with the totem-pole output stage. However, when the output transistor is turned OFF, the output is pulled up to about 5 V by the external resistance (assuming no current is drawn from it).

The open collector output is often used for a wired-OR configuration, when a number of open-collector gates share the same pull-up resistor.

Q19 Identify the circuit shown below. Give one reason why this type of circuit may be used in preference to a transistor-transistor-logic (TTL) circuit. (*2 min*)



A19 The circuit shown is an emitter-coupled logic OR gate. It is used in preference to TTL circuits whenever very-high-speed operation is required.

Questions and answers contributed by D. Turner

[*Tutorial note:* Some questions given below require a knowledge of the mnemonics and machine code of a specific microprocessor. It would clearly be impossible to duplicate all such questions and answers for a range of microprocessors. Therefore, the Zilog Z80 has been chosen as a representative microprocessor because of its widespread use and machine-code compatability with the Intel 8080 and 8085. Students who have studied the Rockwell 6502 or Motorola 6800 should not find too much difficulty in adapting the questions for those microprocessors.]

A shortened instruction set for the Z80 is given below.

Mnemonic	Hexadecimal Code	Comment
LD A, *n*	3E *n*	Load the accumulator (register A) with data *n*.
LD A, B	78	Load the accumulator with the contents of register B.
LD B, *n*	06 *n*	Load register B with data *n*.
LD B, A	47	Load register B from the accumulator.
LD C, A	4F	Load register C from the accumulator.
LD HL, *nn*	21 *nn*	Load register pair HL with the number *nn*.
LD A, (HL)	7E	Load the accumulator from address (HL).
LD (HL), A	77	Load address (HL) from the accumulator.
ADD A, (HL)	86	Add the contents of address (HL) to the accumulator.
ADD A, B	80	Add the contents of register B to the accumulator.
AND B	A0	Logical AND the contents of register B with the contents of the accumulator.
SUB *n*	D6 *n*	Subtract number *n* from the accumulator.
INC HL	23	Increment register pair HL by 1.
INC A	3C	Increment the accumulator by 1.
INC B	04	Increment register B by 1.
DEC HL	2B	Decrement register pair HL by 1.
DEC A	3D	Decrement the accumulator by 1.
DEC B	05	Decrement register B by 1.
JP *nn*	C3 *nn*	Jump to address *nn*.
JP Z *nn*	CA *nn*	Jump on zero to address *nn*.
JP NZ *nn*	C2 *nn*	Jump on non-zero to address *nn*.
HALT	76	Halt.

Note: n is an 8 bit data item; *nn* is a 16 bit data item or address

Q1 *Write down the BINARY and OCTAL equivalents of the following HEXADECIMAL numbers:*

(a) 7AF, and (b) CD. *(4 min)*

A1 [Each number can be converted first to binary by writing down the equivalent binary value for each character.]

(*a*) 7 A F
0111 1010 1111

$\therefore$ 7AF hex = $\underline{011\ 110\ 101\ 111_2}$.

(*b*) C D
1100 1101

$\therefore$ CD hex = $\underline{11\ 001\ 101_2}$.

[The binary values can be converted to octal by grouping the bits in threes starting from the least significant bit.]

(*a*) 011 110 101 111
3 6 5 7

$\therefore$ 7AF hex = $\underline{3657_8}$.

(*b*) 11 001 101
3 1 5

$\therefore$ CD hex = $\underline{315_8}$.

Q2 *Convert the following decimal numbers to their binary equivalent. Show all working.*

(a) 220, and (b) 63. *(5 min)*

A2 [The conversion is performed by repeated division by 2.]

(*a*)

Quotient	Remainder
2) 220	
110	0 LSB
55	0
27	1
13	1
6	1
3	0
1	1
0	1 MSB

LSB: least significant bit MSB: most significant bit

$\therefore$ $220_{10} = \underline{11\ 011\ 100_2}$.

(*b*)

Quotient	Remainder
2) 63	
31	1 LSB
15	1
7	1
3	1
1	1
0	1 MSB

$\therefore$ $63_{10} = \underline{111\ 111_2}$.

Q3 *Explain briefly why hexadecimal or octal numbers are often used by computer programmers.* *(3 min)*

A3 All computers work in binary numbers. However, strings of binary digits are very difficult for a programmer to manipulate and remember so a simpler form of number representation must be used.

Octal numbers can be used to represent groups of 3 binary digits, which means that binary numbers translated to octal are very much easier to remember. Main-frame computer and minicomputer programmers often use octal number representation.

In microcomputer systems, data bytes typically have 8 bits and addresses have 16 bits. Since hexadecimal numbers can be used to represent groups of 4 binary digits, they are very well suited for use in microcomputer programming. The use of hexadecimal numbers also makes the task of data entry in machine code very much easier.

Q4 *Perform the following binary calculations:*

(a) 10 110 + 11 010, and

(b) 1011 + 1001. *(5 min)*

A4 (*a*)

	10 110	(22_{10})
	11 010	(26_{10})
carry	1 1 1 1 0	
sum	110 000	(48_{10})

(*b*)

	1 011	(11_{10})
	1 001	(9_{10})
carry	1 0 1 1	
sum	10 100	(20_{10})

Q5 *Use the method of 'complement addition' to perform the following calculation $1000_2 - 110_2$.* *(3 min)*

A5 First find the 1's complement of 110 by inverting each bit, then add 1 to find the 2's complement, as follows:

	0110
Invert	1001
Add 1	1
2's complement	1010

Subtract by adding the 2's complement, as follows:

	1000
Add	1010
	(1) 0010

The overflow bit (1) indicates that the answer is positive.
Therefore, the result is $+0010$.

Q6 Explain the following terms applied to microcomputer systems:

(*a*) *operator,*

(*b*) *operand,*

(*c*) *FETCH, and*

(*d*) *EXECUTE.* (*4 min*)

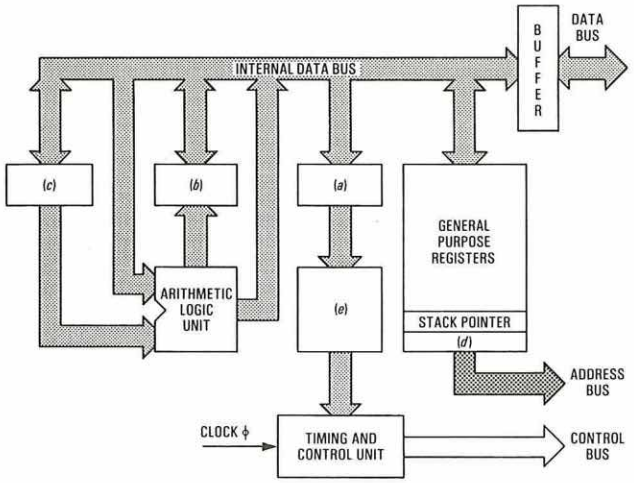
A6 (*a*) The operator is the part of an instruction which defines the operation to be performed. It is sometimes known as the *op-code*.

(*b*) The operand is the part of an instruction which specifies either the actual data or the location of the data to be used in an operation. The data location may be a register, a port or a memory address.

(*c*) FETCH refers to the FETCH part of the FETCH/EXECUTE cycle which every computer operates. During the operation of a program each new instruction has to be retrieved from memory in turn. The FETCH phase is the time when a new op-code is read from memory and placed in the instruction register of the central processing unit.

(*d*) The EXECUTE part of the computer FETCH/EXECUTE cycle refers to the time when each instruction specified by its op-code is actually carried out.

Q7 Write down the names of the blocks marked with the letter (a)–(e) in the diagram below. (*3 min*)



A7 (*a*) The instruction register.

(*b*) The flags or status register.

(*c*) The accumulator.

(*d*) The program counter.

(*e*) The instruction decoder.

Q8 Briefly explain the function of the following in a microprocessor:

(*a*) *arithmetic logic unit,*

(*b*) *general purpose registers,*

(*c*) *control bus, and*

(*d*) *clock.*

(*8 min*)

A8 (*a*) **Arithmetic Logic Unit.**

The arithmetic logic unit (ALU) is a logic circuit within the central processing unit (CPU) where all the arithmetic and logical operations are carried out. The EXECUTE part of all data manipulation instructions, such as ADD, SUBTRACT, AND, OR, COMPARE etc., uses the ALU. Generally there are 2 inputs which hold the operands and one of these is the accumulator. Results produced in the ALU are normally returned to the accumulator, and they can affect some of the flags in the flag register.

(*b*) **General Purpose Registers.**

A microprocessor may or may not have a group of general purpose registers. Where they form part of the CPU they provide a small number of very convenient locations which can be used to store temporary data values awaiting processing. The number of registers available varies from one microprocessor to another.

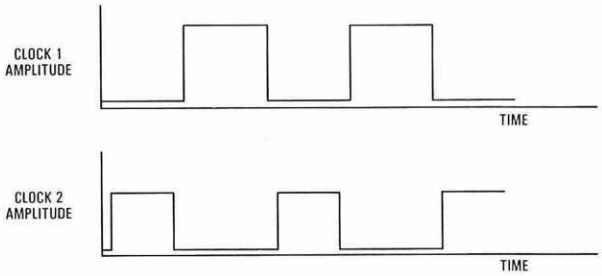
(*c*) **Control Bus.**

The control bus is the collection of wires that carry signals used to synchronise the operation of a microprocessor system. Typical control bus signals include *memory read, memory write, input/output read, input/output write, interrupt, reset, bus request* etc. Some signals are generated by the CPU, whereas others may originate in one of the peripheral devices. Different microprocessors each have their own group of control signals.

(*d*) **Clock.**

The clock is a highly stable oscillator that generates the basic timing signals to which the microprocessor is synchronised. Most clock oscillators are crystal controlled and some microprocessors include the circuit as part of the CPU.

Some systems require a 2-phase clock, as shown in the sketch, whereas others require only a single phase. Typical clock frequencies for a microprocessor are between 1 MHz and 6 MHz.

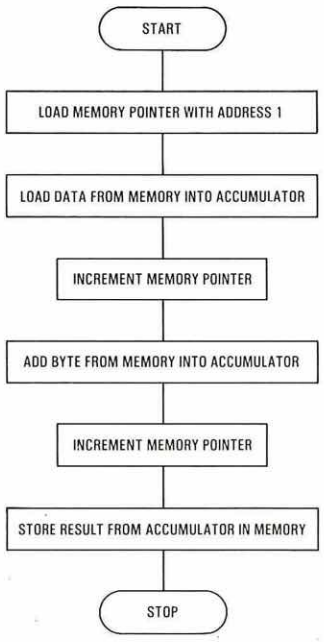


Q9 Name the program which must be resident in a microcomputer system before other programs can be located and executed. (*1 min*)

A9 A monitor program is generally resident in read-only memory in a microcomputer system and is arranged so that it is executed as soon as power is applied. The monitor program then provides the basic operating functions such as keyboard data entry and display facilities, which allow other programs to be entered and executed.

Q10 Draw the flow chart for a program which will add together 2 bytes of data in adjacent memory locations and place the result in the next memory location. (*4 min*)

A10



[*Tutorial note:* This flow chart indicates only one of a number of possible correct solutions to the problem.]

Q11 Use the flow chart from the answer to Q10, to produce a machine-code program for the microprocessor of your choice. Start the program at address 1000 hex and assume that the 2 bytes of data are in addresses 2000 hex and 2001 hex. Present the program under the headings of Address, Hexadecimal Code and Mnemonic.

A11 The program for a Z80 microprocessor is shown below.

Address	Hexadecimal Code	Mnemonic
1000	21	LD HL, 2000 hex
1001	00	
1002	20	
1003	7E	LD A, (HL)
1004	23	INC HL
1005	86	ADD A, (HL)
1006	23	INC HL
1007	77	LD (HL), A
1008	76	HALT

Q12 Draw a trace table showing the contents of the program counter, accumulator, B register and memory address 3000 hex during the execution of the program given in the table below. Initially, memory address 3000 hex contains the data 07 hex and the contents of the accumulator and B register are unknown. *(4 min)*

Address	*Hexadecimal Code*	*Mnemonic*
1030	*3A 00 30*	*LD A, (3000 hex)*
1033	*06 78*	*LD B, 78 hex*
1035	*80*	*ADD A, B*
1036	*D6 0F*	*SUB 0F hex*
1038	*32 00 30*	*LD (3000 hex), A*
103B	*76*	*HALT*

A12

Program Counter	Accumulator	B Register	Address 3000 hex
1030	*X*	*X*	07
1033	07	*X*	07
1035	07	78	07
1036	7F	78	07
1038	70	78	07
103B	70	78	70
103C	70	78	70

X = unknown

Q13 Microprocessor instructions may be classified into 3 main groups. What are they?

Give the mnemonic for one instruction from each group and explain its function. *(5 min)*

A13 Microprocessor instructions may be classified as

(*a*) data movement instructions,
(*b*) data manipulation (arithmetic and logic) instructions, and
(*c*) flow-of-control (test and branch) instructions.

LD B,A is the mnemonic for a typical data movement instruction. Its function is to move the data from the accumulator into the B register of a Z80 microprocessor.

ADD A,B is the mnemonic for a typical arithmetic instruction. Its function is to add the contents of register B to the contents of the accumulator.

JP 1500 hex is the mnemonic for a typical flow-of-control instruction. It causes the program to jump unconditionally to address 1500 hex for its next instruction.

Q14 Explain what is meant by

(*a*) *register addressing,*
(*b*) *indirect addressing,*
(*c*) *immediate addressing, and*
(*d*) *direct addressing.* *(6 min)*

A14 (*a*) **Register Addressing.**

Register addressing is an addressing mode used by instructions which operate wholly upon central-processing-unit (CPU) registers. The source and/or destination registers each have a 3 bit address which forms part of the single byte op-code.

(*b*) **Indirect Addressing.**

Instructions which involve data transfers between CPU and memory may use indirect addressing. A register pair (16 bits) is used to store the memory address which contains the data to be operated upon.

(*c*) **Immediate Addressing.**

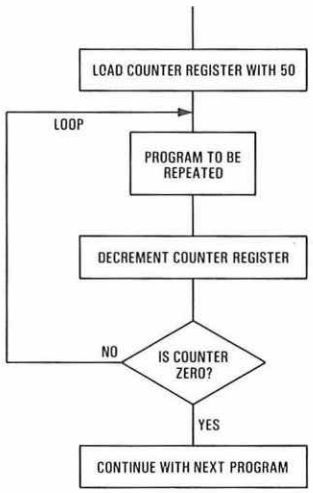
In an instruction which uses immediate addressing, the operand follows in the memory address(es) immediately after the op-code.

(*d*) **Direct Addressing.**

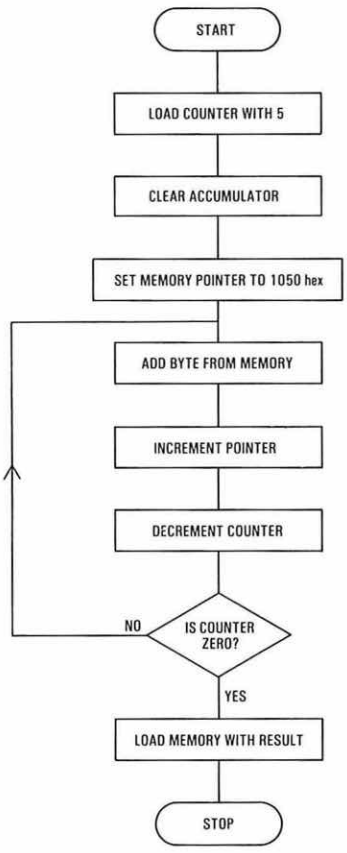
Direct addressing is an addressing mode used for data transfers between CPU and memory. The memory address containing the data to be operated upon is specified in bytes 2 and 3 of the instruction.

Q15 Draw a flow chart to indicate how part of a program can be repeated 50 times. *(3 min)*

A15



Q16 The flow chart below could be used as the basis of a program which adds together 5 numbers stored in sequential memory addresses starting at address 1050 hex. It then puts the result in the next memory address. Use the instruction set provided to produce a machine-code program under the headings Address, Hexadecimal Code and Mnemonic, starting at address 1000 hex. *(8 min)*



A16

Address	Hexadecimal Code	Mnemonic
1000	06	LD B, 05
1001	05	
1002	3E	LD A, 00
1003	00	
1004	21	LD HL, 1050 hex
1005	50	
1006	10	
1007	86	ADD A, (HL)
1008	23	INC HL
1009	05	DEC B
100A	C2	JP NZ 1007 hex
100B	07	
100C	10	
100D	77	LD (HL), A
100E	76	HALT

[*Tutorial note:* Registers C, D or E could be used as the counter register instead of register B.]

Q17 An integrated circuit is described as a '4K × 8 bit ROM'. Explain what this means. (*1 min*)

A17 A *4K × 8 bit ROM* refers to a read-only memory which contains 4096 bytes each with 8 bits of data.

Q18 A memory chip has 10 address pins and 4 data pins. Answer the following.

(*a*) *How many memory locations does it have?*

(*b*) *How many bits of data are stored?*

(*c*) *How many similar chips would be needed to create a 2K × 8 bit memory?* (*5 min*)

A18 (*a*) The number of memory locations is $2^{10} = 1024$ (1K).

(*b*) Each location can store 4 bits.
Therefore the chip contains $1024 \times 4 = 4096$ bits.

(*c*) Four chips each 1K × 4 bit would be required to make up a 2K × 8 bit memory.

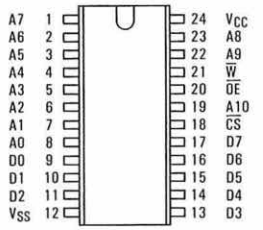
Q19 With reference to the diagram, explain the function of the following pins:

(*a*) $\overline{CS}$,

(*b*) $\overline{W}$,

(*c*) *D0–D7, and*

(*d*) *A0–A10.* (*4 min*)



A19 (*a*) $\overline{CS}$ is an abbreviation for *chip select*. The CS pin has an active LOW signal connected to it which is used to select one chip out of all the memory chips in the system. Normally, the *CS* signal is derived, via a decoder, from the address bus.

(*b*) $\overline{W}$ is an abbreviation for *write*. When the signal is LOW, this indicates that data from the data bus will be written into the chip.

(*c*) D0–D7 indicate the data bus connections to the chip. The least significant bit is D0. Each pin is capable of bidirectional data transfer.

(*d*) A0–A10 indicate the address bus connections to the chip. The least significant bit is A0. Address bus lines are all inputs.

Q20 Complete the following sentence:
The data and address buses differ because . . .

(*a*) *the address bus is bidirectional but the data bus is tri-state.*

(*b*) *the address bus is unidirectional but the data bus is bidirectional.*

(*c*) *the address bus is 'active HIGH' but the data bus is 'active LOW'.*

(*d*) *the address bus is tri-state but the data bus is unidirectional.* (*1 min*)

A20 (*b*) the address bus is unidirectional but the data bus is bidirectional.

Q21 Draw the truth table and explain the function of a tri-state buffer with an 'active LOW' control input. (*5 min*)

A21

Control	Data Input	Output
1	1	X
1	0	X
0	1	1
0	0	0

X—open-circuit

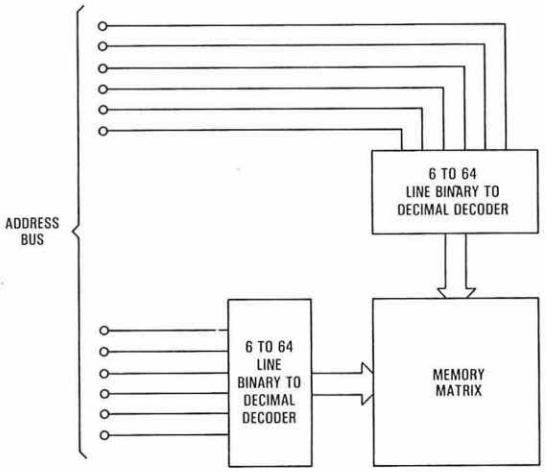
A tri-state buffer is a logic gate which has 3 possible output states: logic 1, logic 0 and open-circuit (high resistance). Its operation can be seen from the truth table above. When its control input is a logic 1, the output is in its open-circuit state irrespective of the condition of the data input. However, when the control input is logic 0, the output has the same logic state as the input.

This type of buffer is used to connect a number of outputs to a common line, such as the data bus in a microprocessor system. When a buffer is not required to provide data for the common bus line, it is put into its open-circuit condition so that it will not interfere with other devices which may be providing data at that moment.

Q22 Briefly describe the function of an address decoder found within a memory chip. (*5 min*)

A22 The address supplied to a memory chip is in binary code. Each memory bit must be capable of being selected uniquely when required, and, therefore, this requires some form of binary-to-decimal decoder.

Since memory cells are normally arranged in a matrix, most memory chips contain 2 binary-to-decimal decoders, as shown below.

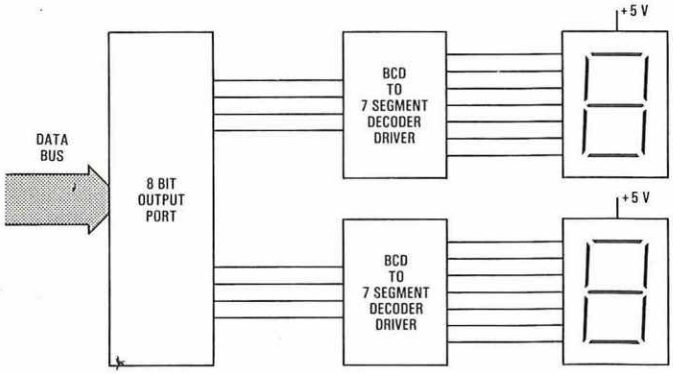


Q23 Briefly describe the problems which must be overcome when an 8 bit output port of a microcomputer is connected to a pair of 7-segment light-emitting-diode displays, without multiplexing being used. (*6 min*)

A23 The connection could be made as shown in the sketch.

The first problem is that each segment of a 7-segment display has to be driven with a current of between 10 and 20 mA. This is much more than the output port could sink, so some form of buffer is required. In addition, two 7-segment displays have 14 connections, so the number of lines available from the port has to be adjusted in some way.

Fortunately, both of these problems can be overcome with the use of



2 binary-coded decimal (BCD) to 7-segment decoder driver circuits. These provide both the electrical buffering and the required number of connections. They also include the necessary code conversion circuits which allow the computer software to simply generate the correct BCD numbers for display rather than having to produce the 7-segment decoded equivalents of them.

Q24 Four of the control lines of the Z80 microprocessor are

(*i*) $\overline{RD}$ (*read*),
(*ii*) $\overline{WR}$ (*write*),
(*iii*) $\overline{MREQ}$ (*memory request*), *and*
(*iv*) $\overline{IOREQ}$ (*input/output request*).

(*a*) *Explain the function of each line.*

(*b*) *Which lines would be active during the fetch and execute phases of the instruction OUT* (*n*),*A ?* (*4 min*)

A24 (*a*) (*i*) $\overline{RD}$ This control line goes LOW whenever data is read into the central processing unit (CPU), irrespective of the source of the data.

(*ii*) $\overline{WR}$ This control line goes LOW whenever data is sent from the CPU to some other part of the system.

(*iii*) $\overline{MREQ}$ This control line goes LOW whenever data is transferred between the CPU and memory, irrespective of the direction of the data transfer.

(*iv*) $\overline{IOREQ}$ This control line goes LOW whenever data is transferred between the CPU and one of the system ports, irrespective of the direction of data transfer.

(*b*) The OUT (*n*),A instruction occupies 2 bytes of memory, the first for the op-code, and the second for the port address *n*.

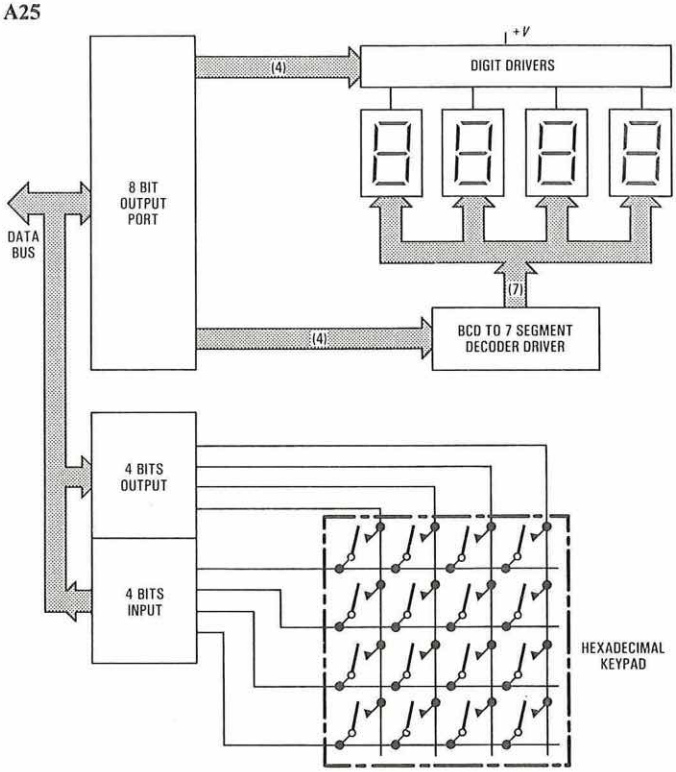
The complete fetch/execute cycle requires 3 machine cycles as shown in

Machine Cycle	Action	Line States
M1	OP-CODE FETCH	$\overline{RD}$ and $\overline{MREQ}$ are active
M2	OPERAND READ	$\overline{RD}$ and $\overline{MREQ}$ are active
M3	WRITE DATA	$\overline{WR}$ and $\overline{IOREQ}$ are active

M2 and M3 constitute the EXECUTE phase of the instruction.

Q25 Draw a block diagram to show how a microcomputer system with output and input ports can be connected to a hexadecimal keyboard and four 7-segment displays. (*6 min*)

A25



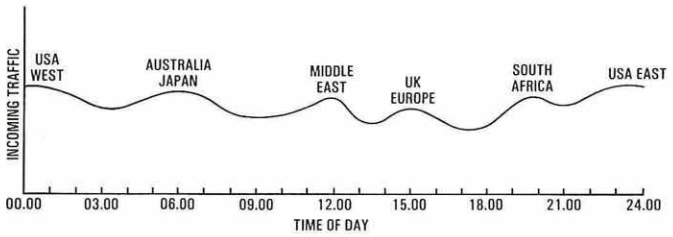
Questions and answers contributed by D. Turner

TEC: TELEPHONE SWITCHING SYSTEMS II

TEC unit number U81/753. Students are advised to read the notes on p. 49

Q1 Sketch a typical graph of traffic against time over a 24 h period for incoming traffic to a Telex exchange catering mainly for international calls. Briefly explain the reason for the shape of your graph. (*15 min*)

A1



Compared with telephone traffic, a much higher proportion of Telex calls go overseas, where the working day is displaced according to the part of the world. As a teleprinter can receive calls automatically, it can receive messages at all times of the day or night. Therefore, a Telex exchange could be receiving incoming traffic over the whole 24 h period. The sketch shows a typical pattern of incoming traffic; some typical sources of traffic are also shown.

Q2 If one telephone circuit is fully occupied for 40 min during the exchange busy hour, is the traffic intensity

(*a*) *0·4 erlangs,*
(*b*) *2400 erlangs,*
(*c*) *0·67 erlangs,*
(*d*) *40 erlangs, or*
(*e*) *1 erlang ?* (*2 min*)

A2 (*c*) 0·67 erlangs.

[*Tutorial note:* Traffic intensity is a measure of circuit occupancy. Thus, if a circuit is occupied for 40 min during the busy hour, then the traffic intensity is 40/60 = 0·67 erlangs.]

Q3 The grade of service in a telephone exchange is given by... (Select the correct answer from the following list.)

(*a*) *the number of calls lost × the number of calls offered.*
(*b*) *traffic lost × traffic offered.*
(*c*) $\dfrac{\textit{traffic carried}}{\textit{traffic lost}}$.
(*d*) $\dfrac{\textit{calls lost}}{\textit{calls offered}}$. (*1 min*)

A3 (*d*) $\dfrac{\text{calls lost}}{\text{calls offered}}$.

Q4 Indicate whether the following statements are true or false. All the statements refer to a 5-digit Strowger non-director exchange. (*5 min*)

(*a*) *Dial tone is returned from the first group selector.* *TRUE/FALSE*

(*b*) *Excluding the customer's uniselector, 5 switching stages are required.* *TRUE/FALSE*

(*c*) *If all the outlets on a group-selector level are engaged, the selector returns number-unobtainable tone.* *TRUE/FALSE*

(*d*) *If the called customer is free, ring tone is returned to the calling customer from the final selector.* *TRUE/FALSE*

(*e*) *The calling customer's meter is operated as soon as dialling is completed.* *TRUE/FALSE*

A4 (*a*) True.

(*b*) False.

[*Tutorial note:* The final selector accepts the last 2 dialled digits and hence only 4 switching stages are required.]

(*c*) False.

[*Tutorial note:* If all the outlets on any level are engaged, the selector automatically makes an eleventh rotary step and returns *equipment-engaged* tone from the eleventh-step bank contact.]

(*d*) True.

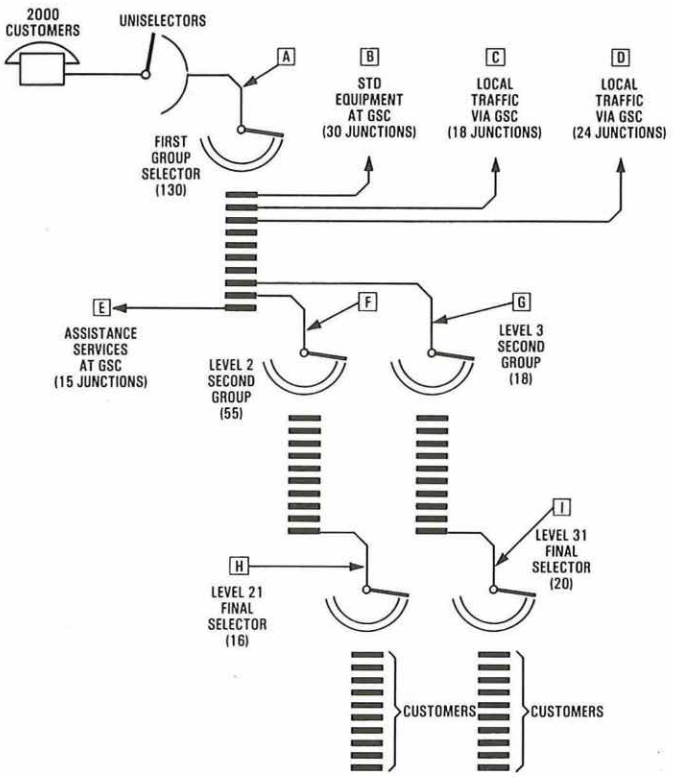
(*e*) False.

[*Tutorial note:* Metering starts only when the called customer answers.]

Q5 *Indicate in the table provided whether full or limited availability exists at the points indicated on the trunking diagram shown below. Assume that 200-outlet 2-motion selectors and 23-outlet uniselectors are being used.*

A		*F*	
B		*G*	
C		*H*	
D		*I*	
E			

Insert F for full availability, or L for limited availability.
(*5 min*)



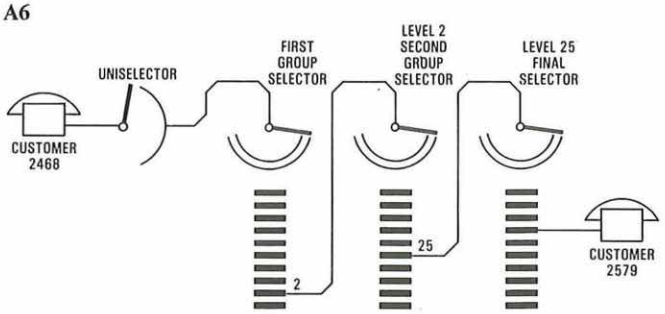
GSC · Group switching centre
Equipment quantities shown in brackets

A5

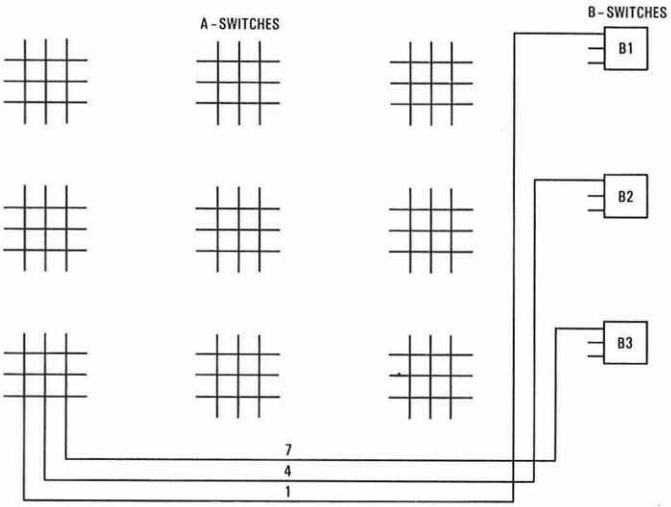
A	L	F	L
B	L	G	F
C	F	H	F
D	L	I	F
E	F		

Q6 *Sketch a simple trunking diagram showing the routeing of a call between customer number 2468 (calling customer) and customer 2579 (called customer) on a Strowger non-director exchange. Label all selectors and levels used.* (*10 min*)

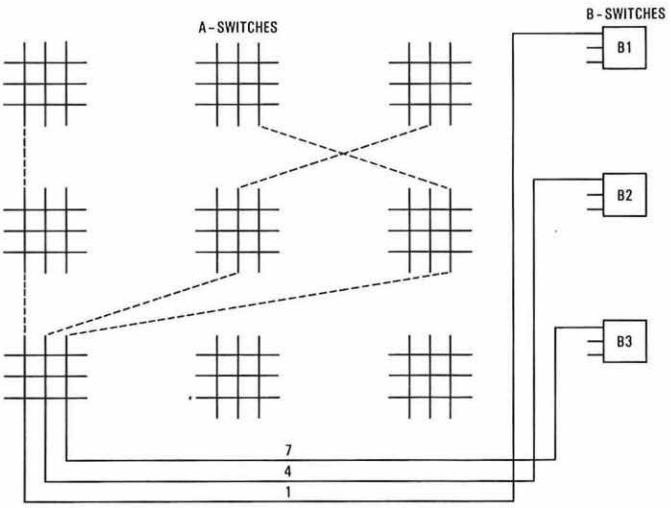
A6



Q7 *A group of A-switches with links to a group of B-switches is shown below. For links 1, 4 and 7, draw in the slipped-multiple arrangement within the A-switch matrix.* (*5 min*)



A7



Q8 *For each part (a)–(e) select, from the list of alternatives, the answer that correctly completes the statement given. All parts refer to a Strowger director exchange.*

(*a*) *A director system...*

(*i*) *reduces the length of a customer's telephone number.*
(*ii*) *standardises dialling codes throughout an area.*
(*iii*) *increases the possible number of customers in an area.*
(*iv*) *makes the routeing of calls quicker.*

(*b*) *A director-area telephone number consists of...*

(*i*) *3 routeing digits and 4 numerical digits.*
(*ii*) *4 routeing digits and 3 numerical digits.*
(*iii*) *7 numerical digits.*
(*iv*) *7 routeing digits.*

(*c*) *The first code selector...*

(*i*) *returns dialling tone to the calling customer.*
(*ii*) *steps to the first digit dialled by the calling customer.*
(*iii*) *routes the call through to the director equipment.*
(*iv*) *steps to the first translated routeing digit pulsed out by the director.*

(*d*) *The maximum number of routeing digits pulsed out by the director is...*

(*i*) *3.*
(*ii*) *4.*
(*iii*) *5.*
(*iv*) *6.*

(*e*) *The director equipment changes some of the dialled digits to...*

(*i*) *numerical digits.*
(*ii*) *code digits.*
(*iii*) *routeing digits.*
(*iv*) *metering digits.* (*5 min*)

A8 (*a*) (*ii*) standardises dialling codes throughout an area.

(*b*) (*i*) 3 routeing digits and 4 numerical digits.

(*c*) (*iv*) steps to the first translated routeing digit pulsed out by the director.

(*d*) (*iv*) 6.

(*e*) (*iii*) routeing digits.

Q9 Explain the main functions of the calling-number generator in a TXE2 electronic telephone exchange. (*5 min*)

A9 When a calling customer originates a call, it is necessary to establish the identity of the calling line so that the common control equipment can find it, and then to transfer that identity in coded form into a selected register. The identification, selection of a register and transfer of the coded information is carried out by the calling-number generator.

Q10 In a TXE2 electronic telephone exchange, the path from the calling customer's line circuit to the register is via... (*Select the correct answer from the following list.*)

(*a*) *A-, B-, and C-switches.*

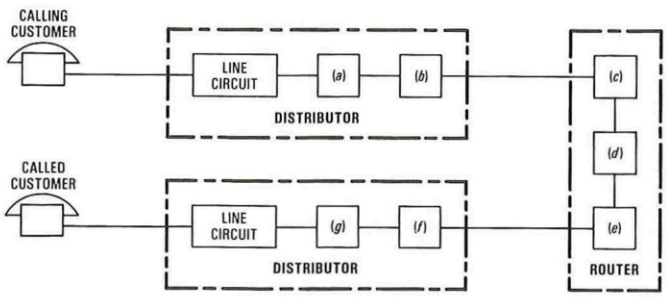
(*b*) *A-, B-, C-, and D-switches.*

(*c*) *A-, B-, and C-switches, and a supervisory relay-set.*

(*d*) *A-, B-, C-, and D-switches, and a supervisory relay-set.* (*1 min*)

A10 (*c*) A-, B-, and C-switches, and a supervisory relay-set.

Q11 The call path of an established call in a TXK1 crossbar telephone exchange is shown below. Name the items labelled (*a*)–(*g*). (*5 min*)



A11 (*a*) Distributor switch B (DSB).

(*b*) Distributor switch A (DSA).

(*c*) Local transmission relay group (LTRG).

(*d*) Router switch A (RSA).

(*e*) Router switch B (RSB).

(*f*) DSA.

(*g*) DSB.

Q12 List 3 functions of a local transmission relay group in a TXK1 crossbar telephone exchange. (*5 min*)

A12 Any 3 from the following:

(*a*) provides ringing current,

(*b*) provides ringing tone,

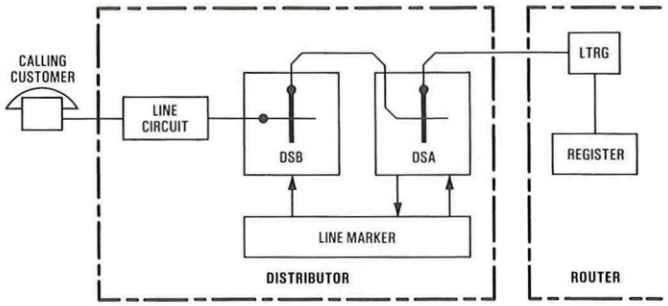
(*c*) provides the transmission bridge, or

(*d*) provides metering.

Q13 With the aid of a suitable diagram, describe the sequence of events leading up to the return of dial tone when a customer on a TXK1 crossbar telephone exchange originates a call. (*20 min*)

A13 The main items of equipment involved are shown in the block diagram.

When the customer lifts his handset, the telephone loop is detected by the line circuit, which alerts the line marker associated with the calling customer's distributor. The line marker instructs the distributor switch B (DSB) connected to the calling customer to look for a free circuit to a distributor switch A (DSA) by sending out marks on all DSA–DSB links. Every DSB has a link to each DSA, and, when a free link is found, the particular DSA is instructed by the line marker to select a free local transmission relay group (LTRG). The selected LTRG must have a link to a free register, and, when an LTRG and



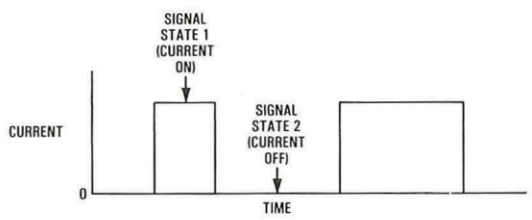
free register have been reserved, a signal is returned to the line marker to indicate that a complete path is available between calling customer and register. On receipt of this signal, the line marker instructs the DSA to operate its selected cross-point. This is followed by the operation of the selected cross-point in the DSB and the completion of the circuit through to the line circuit. The calling customer's loop is now extended to seize the register, which then returns dial tone. The line marker releases and can be used to set up another call from another customer on the distributor.

Q14 Explain what is meant by the term 'link trunking'. (*7 min*)

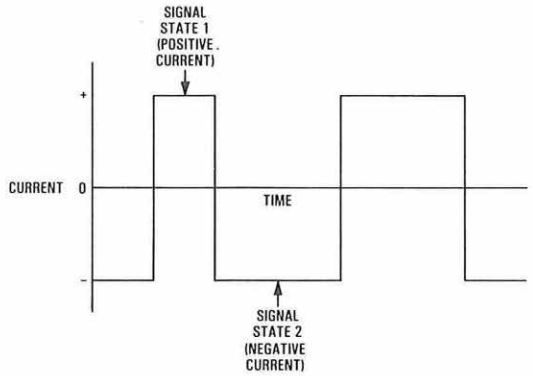
A14 Link trunking is a means of increasing switch efficiency by using several small switch matrices, rather than a single one, in 2 or more stages. The outlets of one stage are connected to the inlets of the next stage by means of connecting links. With this method, the number of crosspoints required to interconnect a certain number of inlets and outlets can be reduced.

Q15 With the aid of simple signal diagrams, explain the difference between single-current and double-current signalling. (*15 min*)

A15 In a single-current signalling system, information is conveyed by 2 signalling states: current ON and current OFF (see sketch (*a*)). In a double-current system, current is always flowing though not always in the same direction; the 2 signalling states are represented by the direction of the current (see sketch (*b*)).



(*a*)



(*b*)

Q16 *One of the main advantages of multi-frequency signalling compared with Strowger 10 pulses/s signalling is its high speed. Calculate the transmission time for sending the digits 989 using*

(*a*) *nominal 10 pulses/s signalling with an inter-digit pause of 800 ms, and*

(*b*) *multi-frequency signalling with an 80 ms signal period and an 80 ms inter-digit pause.* (*10 min*)

A16 (*a*) 10 pulse/s signalling.

	Time (ms)
digit 9	900
digit 8	800
digit 9	900
2 inter-digit pauses	1600
	4200 = 4·2 s.

(*b*) Multi-frequency signalling

	Time (ms)
digit 9	80
digit 8	80
digit 9	80
2 inter-digit pauses	160
	400 = 0·4 s.

Q17 *One reason why double-current signalling is superior to single-current signalling is... (Select the correct answer from the following.)*

(*a*) *that only a single-wire circuit is needed.*

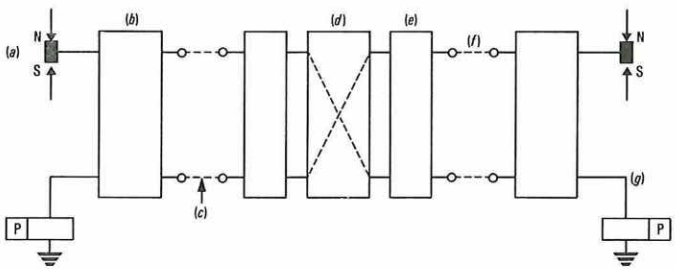
(*b*) *that double-current signals are generated by all telephone dials.*

(*c*) *that there is less signal distortion.*

(*d*) *that the transmit and receive devices are simpler.* (*1 min*)

A17 (*c*) that there is less signal distortion.

Q18 *The block diagram shows a Telex connection between 2 customers, A and B. Name each of the components labelled (a)–(g).* (*10 min*)



A18 (*a*) Transmitter contacts.

(*b*) Line signalling unit.

(*c*) Receive wire.

(*d*) Telex exchange switching equipment.

(*e*) Station line circuit.

(*f*) Send wire.

(*g*) Receive relay.

Q19 *For each part (a)–(d), select, from the list of alternatives, the answer that correctly completes the statement given. All parts refer to a TXK3 crossbar telephone exchange.*

(*a*) *Customers' lines are permanently connected to one side of...*

(*i*) *group selection units.*
(*ii*) *marker units.*
(*iii*) *local selection units.*
(*iv*) *registers.*

(*b*) *Dial pulses are stored in the register via...*

(*i*) *a coupler.*
(*ii*) *an information highway.*
(*iii*) *a group-selection-unit marker.*
(*iv*) *a register junctor.*

(*c*) *A transmission bridge is contained in...*

(*i*) *the group selection units.*
(*ii*) *the call timing junctor.*
(*iii*) *the register.*
(*iv*) *the local feed junctor.*

(*d*) *The group-selection-unit marker routes the call through the unit using...*

(*i*) *1 selection digit.*
(*ii*) *2 selection digits.*
(*iii*) *3 selection digits.*
(*iv*) *2 routeing digits.* (*5 min*)

A19 (*a*) (*iii*) local selection units.

(*b*) (*iv*) a register hunter.

(*c*) (*iv*) the local feed junctor.

(*d*) (*ii*) 2 selection digits.

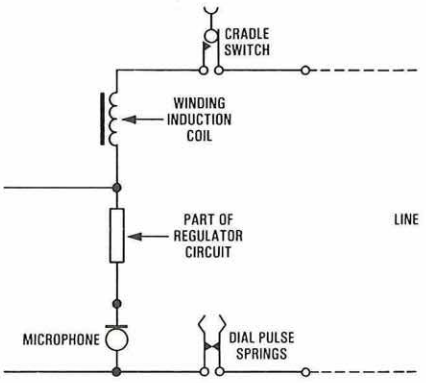
Q20 *Explain the functions of the dial off-normal contacts in a telephone circuit.* (*7 min*)

A20 One set of contacts short circuits the transmitter during dialling; this reduces the resistance in the dialling loop and protects the microphone from damage due to current surges.

A second set of contacts short circuits the receiver during dialling; this prevents dial clicks in the receiver.

Q21 *Sketch and label a circuit showing the components of a modern telephone involved in calling the exchange when the handset is raised.* (*10 min*)

A21



CORRECTIONS

The TEC unit number for Telephone Switching Systems II given on p. 53 of the October 1982 issue of the *Supplement* should have been given as U81/753. The TEC unit number for Telephone Switching Systems III given on p. 73 of the January 1983 issue of the *Supplement* should have been given as U81/745.

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